

U.S.S.N. 09/686,742

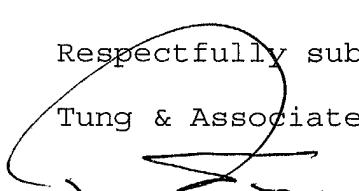
Based on the foregoing, the Applicants respectfully submit that all of the pending claims, i.e. claims 2 and 26-33, are now in condition for allowance. Such favorable action, together with the passage to issuance of the allowed claims 1 and 3-14, is respectfully solicited.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned "Version With Markings To Show Changes Made".

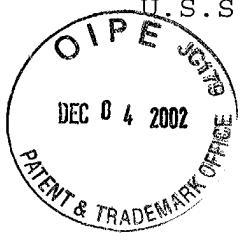
In the event that the present invention is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

Tung & Associates


Randy W. Tung
Reg. No. 31,311
Telephone: (248) 540-4040

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

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In The Specification

Page 12, after paragraph description for Figure 3, please add the following new paragraph:

Figure 3A is an enlarged, cross-sectional view of another embodiment of the present invention electronic structure having a third insulating layer deposited on top.

Page 23, lines 1-17, has been amended as follows:

In another embodiment of the present invention, more than one level of the electrically resistive vias may be formed and connected to each other. For instance, [while not shown in the drawings,] as shown in Figure 3A, a third insulating material layer 66 may be deposited overlying the second plurality of conductive elements and the second insulating material layer; and then a second plurality of electrically resistive vias that have a resistivity of at least 100 $\Omega\text{-cm}$ may be formed in the

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third insulating material layer wherein each of the second plurality of conductive elements is in electrical communication with at least one of the second plurality of electrically resistive vias; and a third plurality of conductive elements is then formed on top of the third insulating material layer each in electrical communication with at least one of the second plurality of electrically resistive vias, whereby at least one of the second plurality of electrically resistive vias is in electrical communication with at least one of the first plurality of electrically resistive vias.

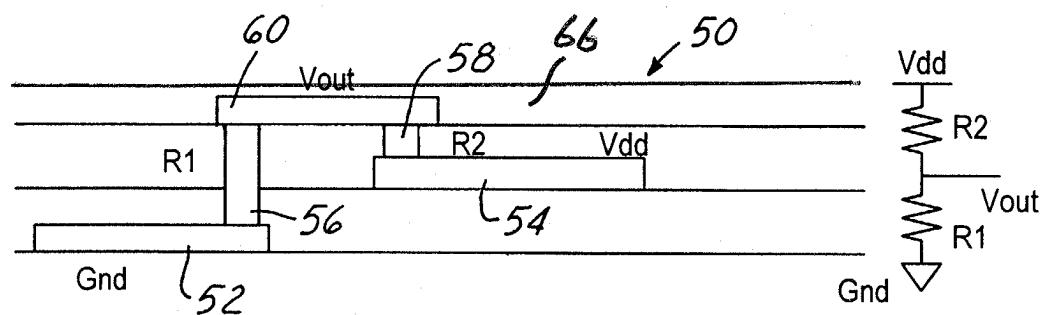


FIG. 3A